EAST - [09943134 tunnel barrier PGPUB.wsp]

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L21: (14) ("6730575" "6514842" "6377070" "5959465" "5488612" "4939559" "4688078").pn.
L22: (13) 09/943134
Failed
Saved
(81) ((asymmetri$4 differen$3) near9 tunnel$3) with (metal perovskite superlattice)
(12804) (float$3 adj gate) same (control adj gate)
(1) (((asymmetri$4 differen$3) near9 tunnel$3) with (metal perovskite superlattice)
(1) (((asymmetri$4 differen$3) near9 tunnel$3) with (metal perovskite superlattice)
(5) (((asymmetri$4 differen$3) near9 tunnel$3) with (metal perovskite superlattice)
(273) ((asymmetri$4 differen$3) near9 tunnel$3) with (oxide)
(203) ((float$3 adj gate) same (control adj gate)) and (((asymmetri$4 differen$3) near9 tunnel$3...
(12) ((asymmetri$4 differen$3) near9 tunnel$3) with (transition$3)
(0) 10/081818
(1632) ald (atomic adj layer adj deposit$3)
(22231) float$3 adj gate
(32840) control adj gate
(13057) (float$3 adj gate) same (control adj gate)
(0) ((float$3 adj gate) same (control adj gate)) same (ald (atomic adj layer adj deposit$3))
(21) ((float$3 adj gate) same (control adj gate)) and (ald (atomic adj layer adj deposit$3))

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DBs | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | Plurals

Default operator: OR | Highlight all hit terms initially

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	D	+/-	Inventor	Document ID	Issue Date	Page	Title	Current OR	Current XRef
1	P		Bhattacharyya, Arup	US 20030151948 A1	20030814	33	Asymmetric band-gap engineered nonvolatile memory device	365/185.18	
2	P		Bhattacharyya, Arup	US 6784480 B2	20040831	32	Asymmetric band-gap engineered nonvolatile memory device	257/314	257/318
3			Eldridge, Jerome M. et al.	US 20040158863 A1	20040819	39	Graded composition metal oxide tunnel barrier interpoly insulators	257/239	
4			Eldridge, Jerome M. et al.	US 20030048666 A1	20030313	39	Graded composition metal oxide tunnel barrier interpoly insulators	365/185.28	257/E21.683; 257/E27.103;
5			Eldridge, Jerome M. et al.	US 20030045082 A1	20030306	33	Atomic layer deposition of metal oxide and/or low asymmetrical tunnel barrier interploy insulators	438/593	257/E21.683; 257/E27.103;
6	P		Forbes, Leonard	US 20040190342 A1	20040930	25	DRAM cells with repressed floating gate memory, low tunnel barrier interpoly insulators	365/185.25	
7	P		Forbes, Leonard	US 20040168145 A1	20040826	33	Service programmable logic arrays with low tunnel barrier interpoly insulators	716/17	326/47
8	P		Forbes, Leonard	US 20040160830 A1	20040819	27	DRAM cells with repressed floating gate memory, low tunnel barrier interpoly insulators	365/185.28	
9	P		Forbes, Leonard	US 6754108 B2	20040622	26	DRAM cells with repressed floating gate memory, low tunnel barrier interpoly insulators	365/185.25	365/149; 365/185.08;
10	P		Forbes, Leonard et al.	US 20040164342 A1	20040826	31	Integrated circuit memory device and method	257/316	

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